Cyclone III Edition

Revision History		
Rev	**Date**	**Description**
A	05 JULY 2007	1) Initial production release.

Schematic Page Description	
Page	**Description**
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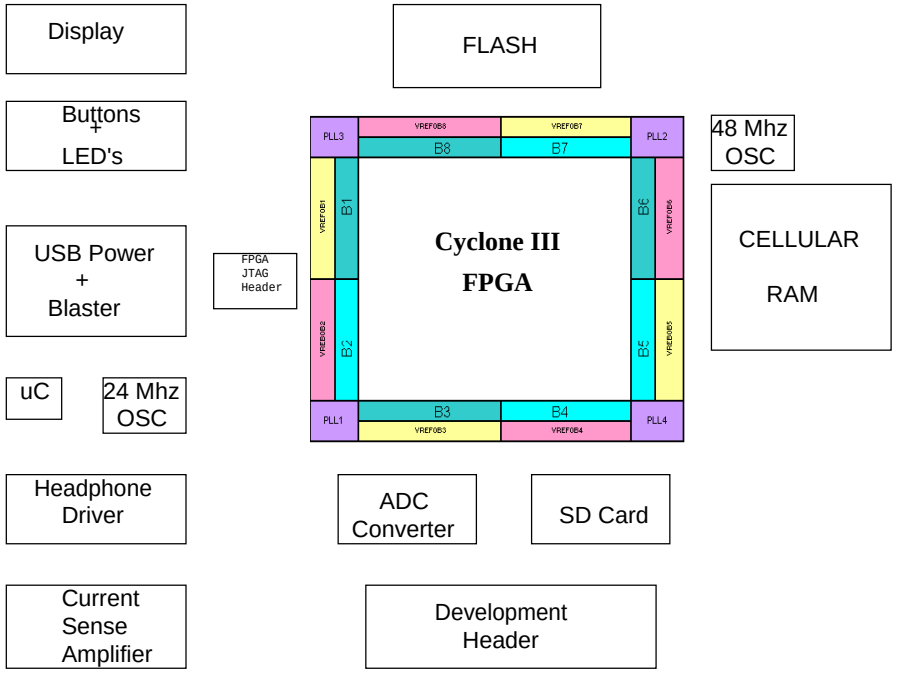
03	Altera FPGA2 - Banks 3 & 4
04	Altera FPGA3 - Banks 5 & 6
05	Altera FPGA4 - Banks 7 & 8
06	Altera FPGA5 - Power & JTAG
07	Clocks
08	Memory
09	Microcontroller
10	ADC Circuit
11	USB Blaster
12	USB Power / Battery Charger
13	Power
14	Audio / Display / IO
15	Miscellaneous

LPRP - Low Power Reference Board



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Low Power Reference Platform
Cover Sheet

Size	CAGE Code	Drawing Number	Rev
B		707-0005	A

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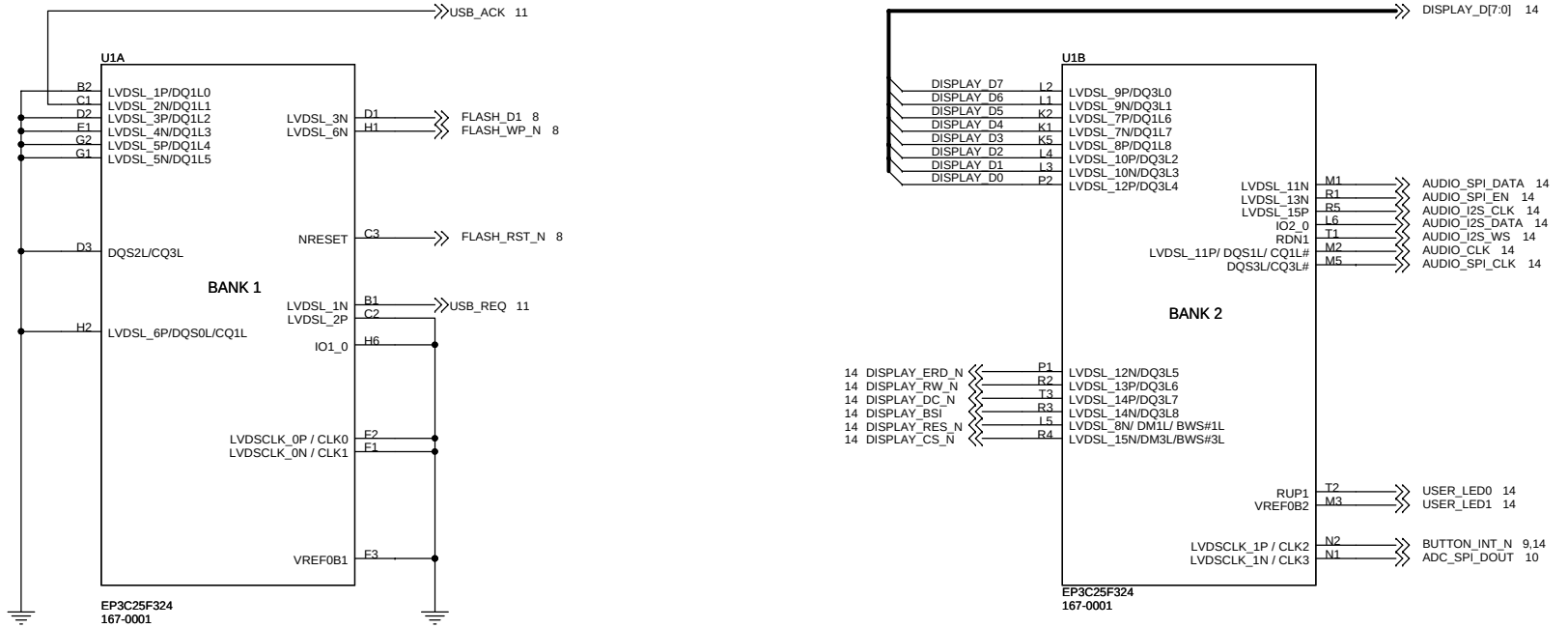
Altera FPGA: Banks 1 & 2



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Altera FPGA - Banks 1 & 2

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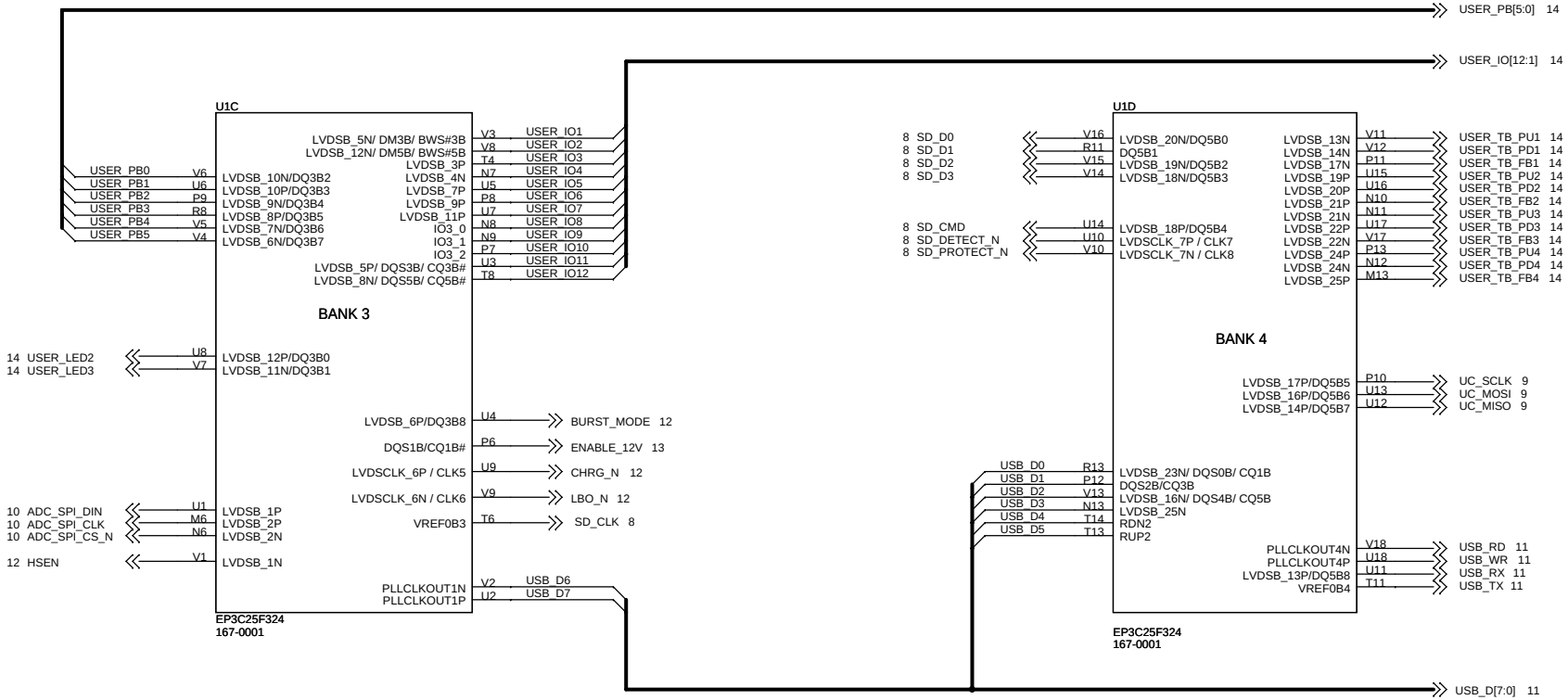
Altera FPGA: Banks 3 & 4



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Altera FPGA - Banks 3 & 4

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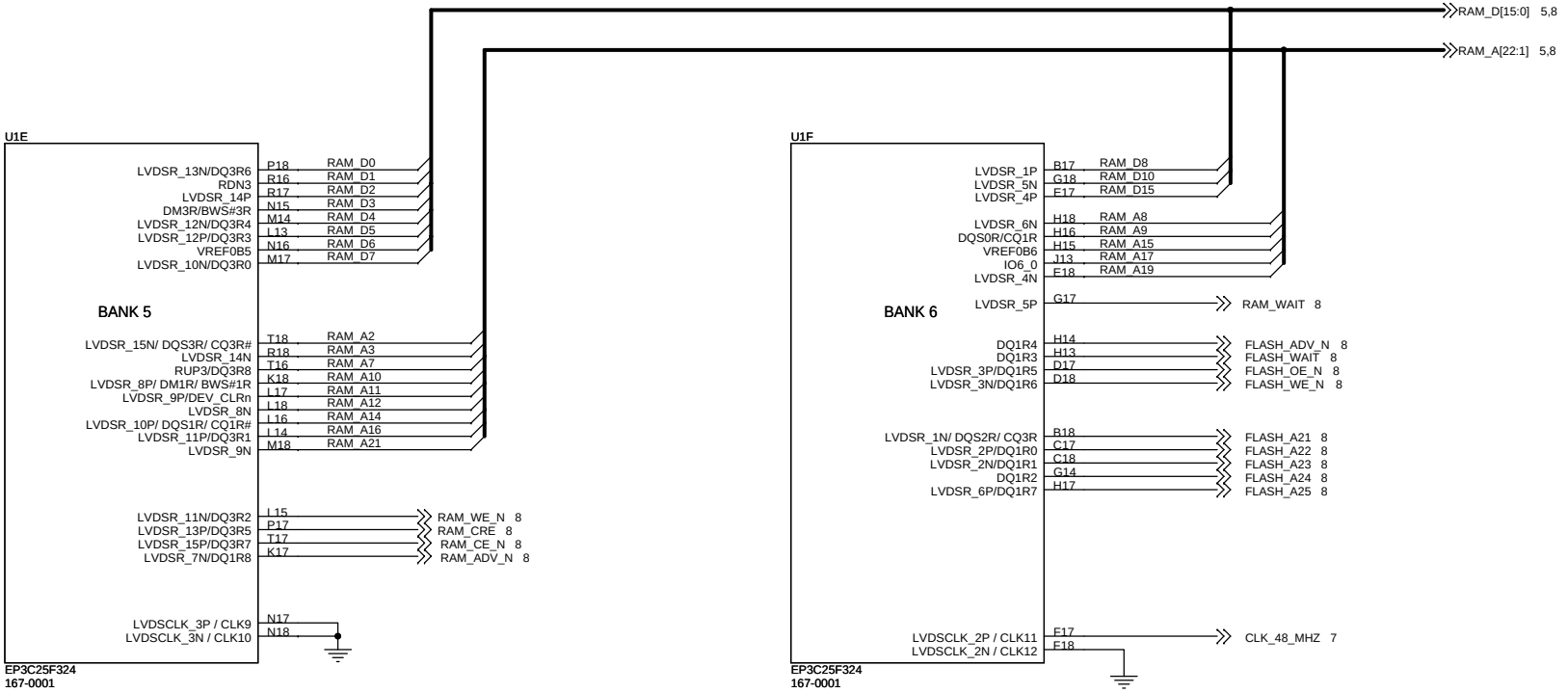
Altera FPGA - Banks 5 & 6



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Altera FPGA - Banks 5 & 6

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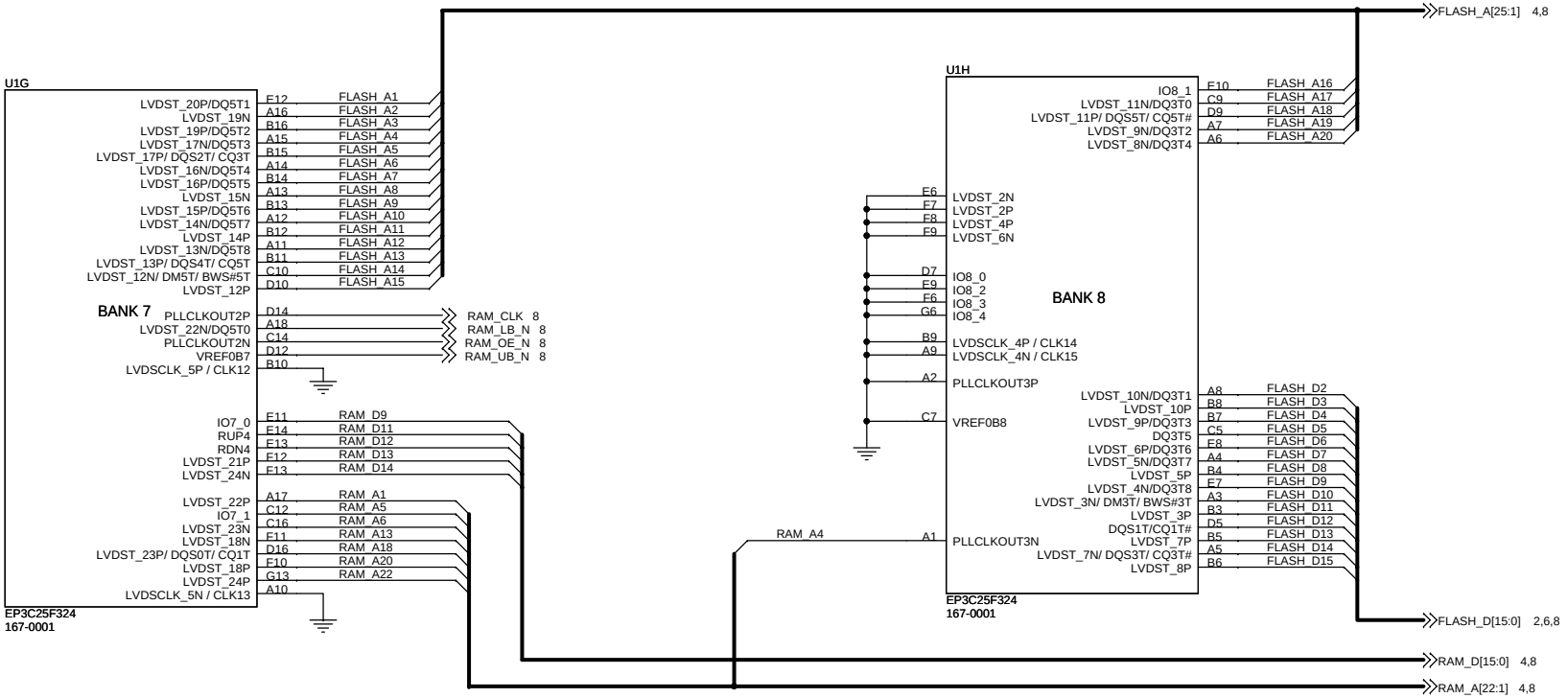
Altera FPGA - Banks 7 & 8



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Altera FPGA - Banks 7 & 8

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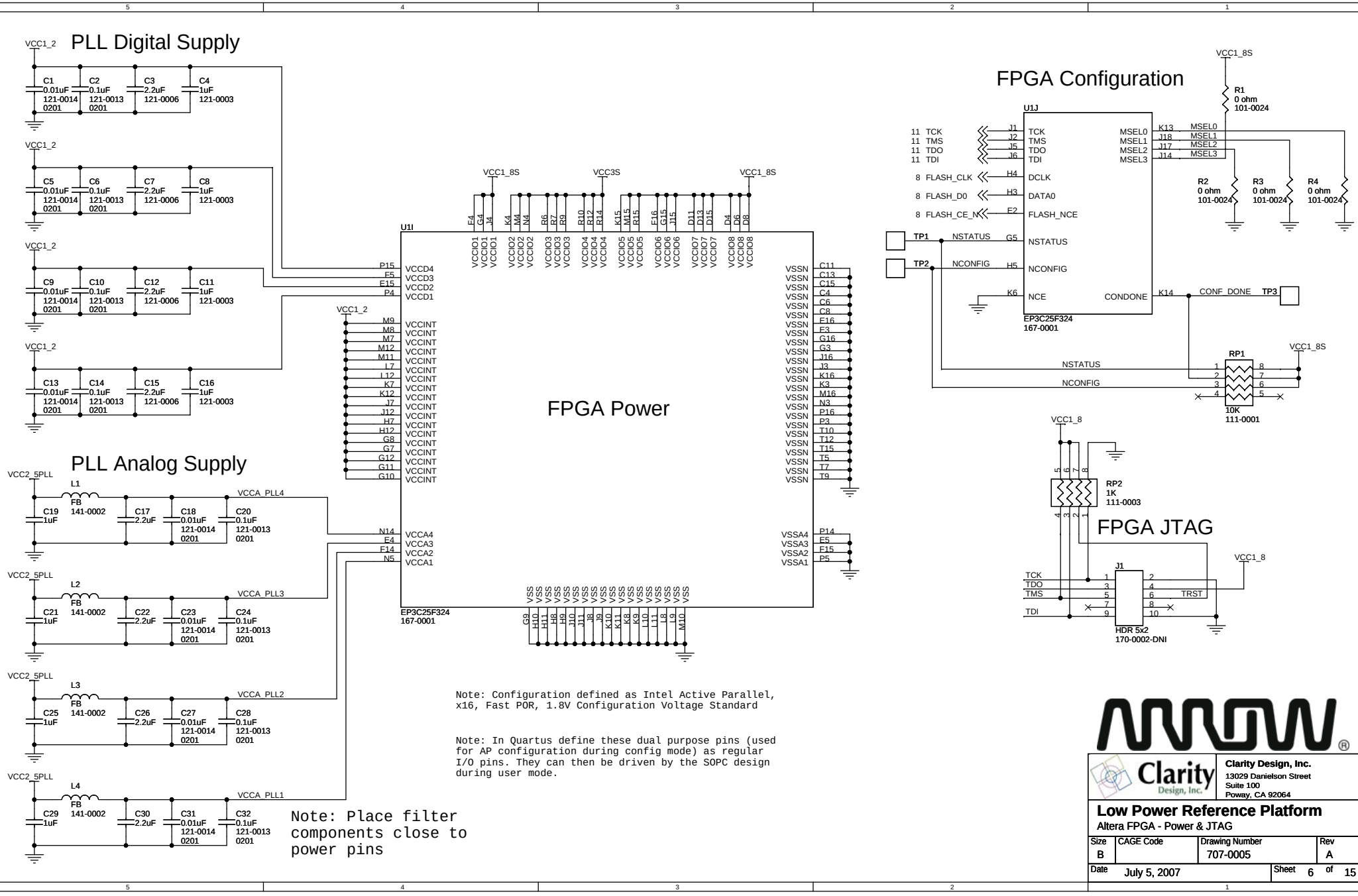
PLL Digital Supply
VCC1_2
C1 0.01uF 121-0014 0201
C2 0.1uF 121-0013 0201
C3 2.2uF 121-0006
C4 1uF 121-0003
C5 C6 C7 C8
C9 C10 C12 C11
C13 C14 C15 C16
PLL Analog Supply
VCC2_5PLL
L1 FB 141-0002
L2 FB 141-0002
L3 FB 141-0002
L4 FB 141-0002
C19 1uF
C17 2.2uF
C18 0.01uF 121-0014 0201
C20 0.1uF 121-0013 0201
C21 1uF
C22 2.2uF
C23 0.01uF 121-0014 0201
C24 0.1uF 121-0013 0201
C25 1uF
C26 2.2uF
C27 0.01uF 121-0014 0201
C28 0.1uF 121-0013 0201
C29 1uF
C30 2.2uF
C31 0.01uF 121-0014 0201
C32 0.1uF 121-0013 0201
VCCA_PLL4
VCCA_PLL3
VCCA_PLL2
VCCA_PLL1
Note: Place filter components close to power pins
FPGA Power
U1I
VCC1_8S
VCC3S
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
P15 VCCD4
F5 VCCD3
E15 VCCD2
P4 VCCD1
M9 M8 M7 M12 M11 L7 L12 K7 K12 J7 J12 H7 H12 G8 G7 G12 G11 G10 VCCINT
N14 VCCA4
E4 VCCA3
F14 VCCA2
N5 VCCA1
C11 C13 C15 C4 C6 C8 F16 F3 G16 G3 J16 J3 K16 K3 M16 N3 P16 P3 T10 T12 T15 T5 T7 T9 VSSN
P14 VSSA4
E5 VSSA3
F15 VSSA2
P5 VSSA1
VSS
EP3C25F324
167-0001
Note: Configuration defined as Intel Active Parallel, x16, Fast POR, 1.8V Configuration Voltage Standard
Note: In Quartus define these dual purpose pins (used for AP configuration during config mode) as regular I/O pins. They can then be driven by the SOPC design during user mode.
FPGA Configuration
U1J
11 TCK
11 TMS
11 TDO
11 TDI
8 FLASH_CLK
8 FLASH_D0
8 FLASH_CE_N
TCK
TMS
TDO
TDI
DCLK
DATA0
FLASH_NCE
TP1 NSTATUS
TP2 NCONFIG
NSTATUS
NCONFIG
NCE
CONDONE
MSEL0
MSEL1
MSEL2
MSEL3
CONF_DONE
TP3
EP3C25F324
167-0001
R1 0 ohm 101-0024
R2 0 ohm 101-0024
R3 0 ohm 101-0024
R4 0 ohm 101-0024
RP1 10K 111-0001
RP2 1K 111-0003
FPGA JTAG
J1
TRST
HDR 5x2
170-0002-DNI
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Low Power Reference Platform
Altera FPGA - Power & JTAG
Size B
CAGE Code
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Date July 5, 2007
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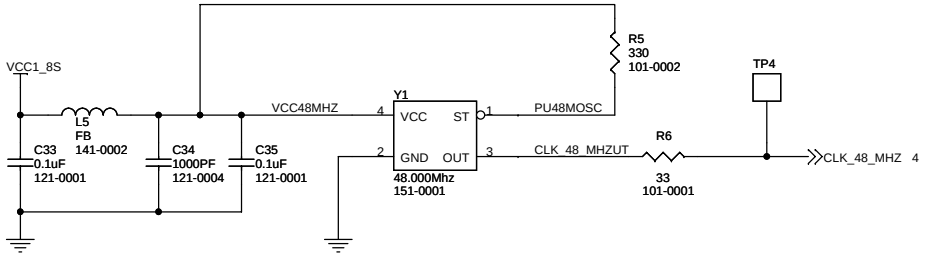
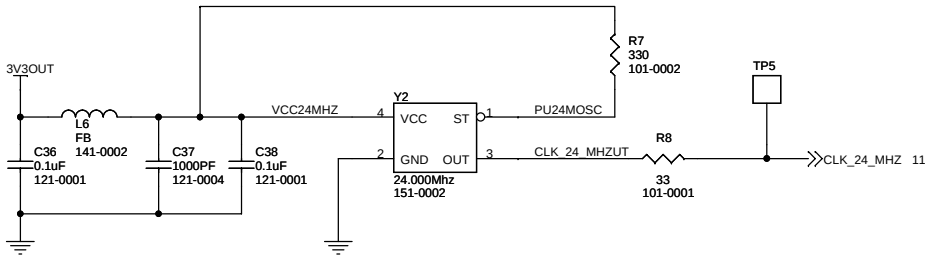
FPGA CLOCK



CPLD CLOCK



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CLOCKS

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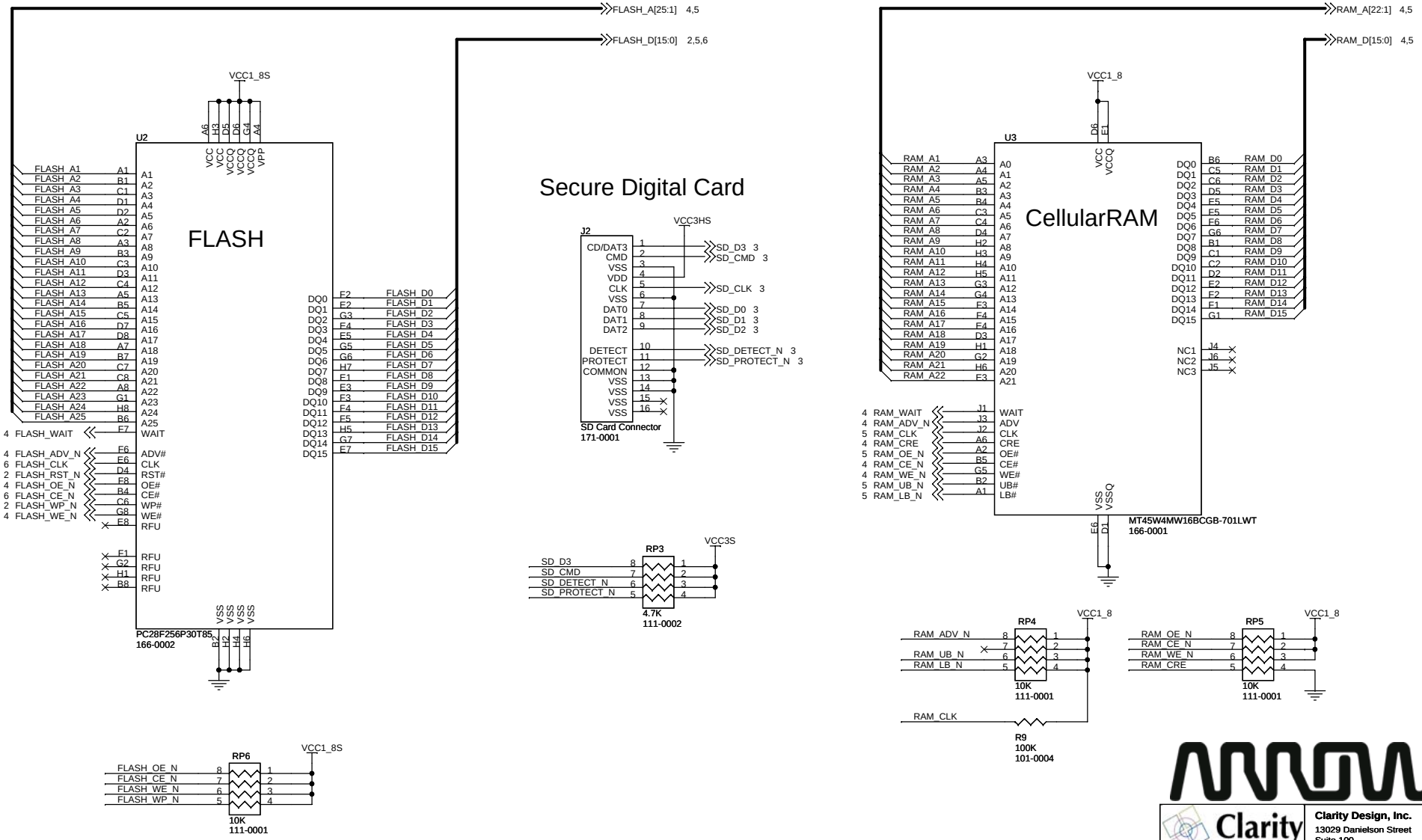

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MEMORY

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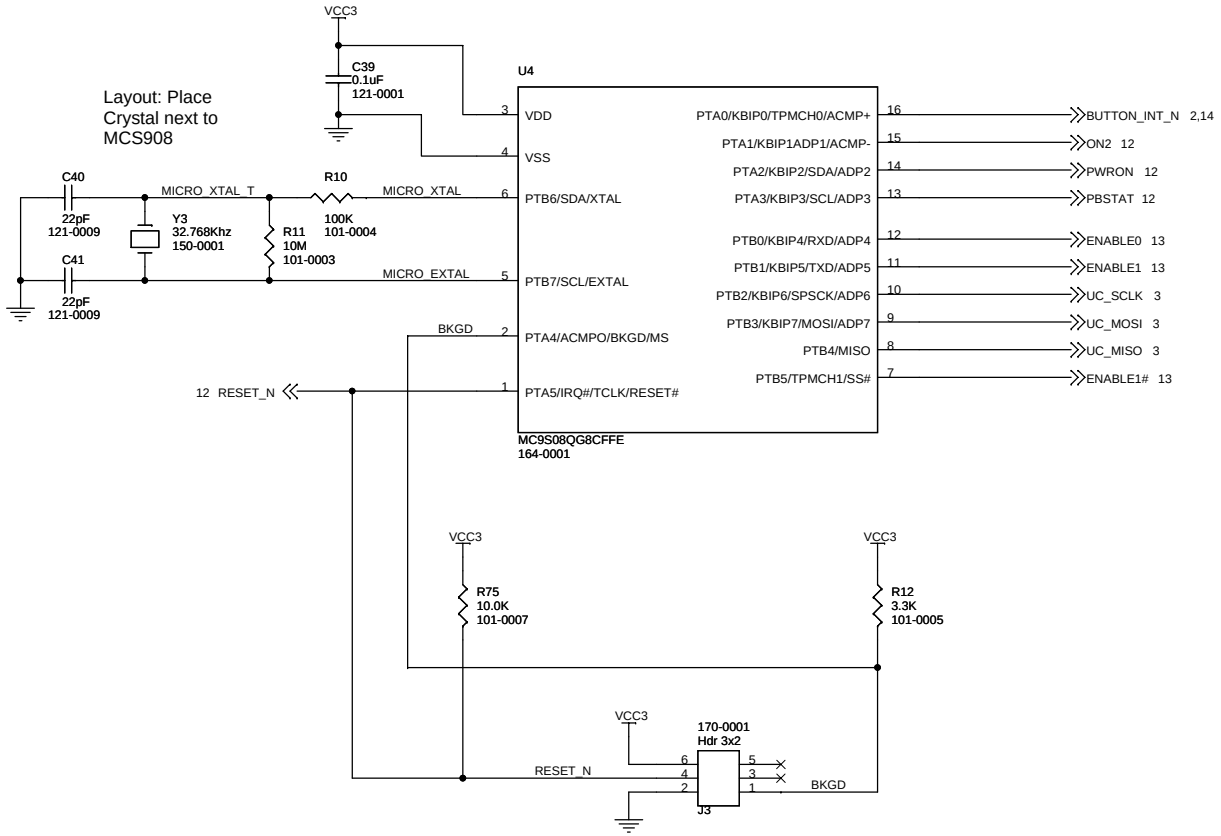
MICROCONTROLLER



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MICROCONTROLLER

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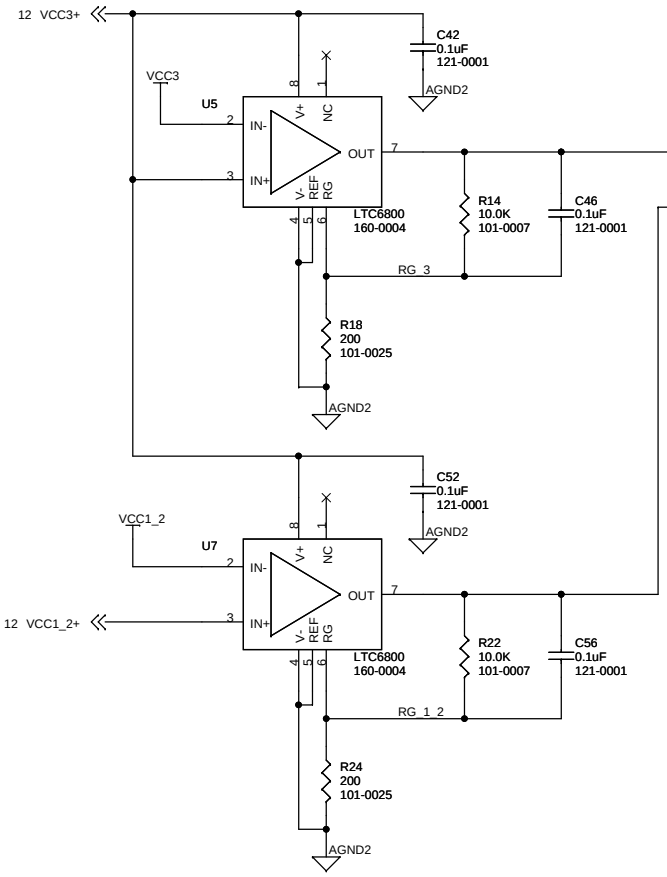
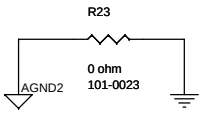
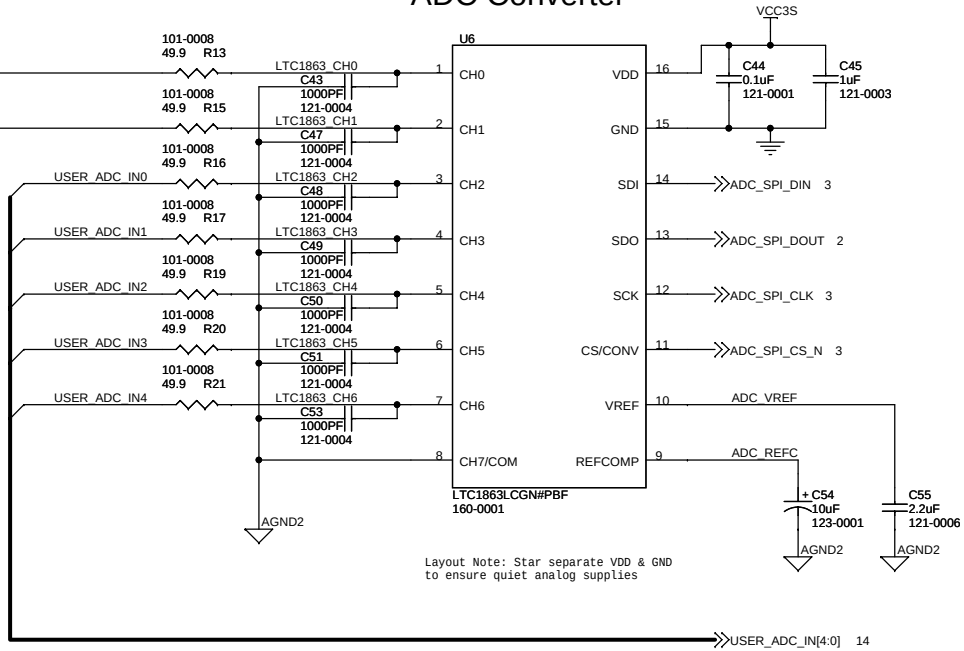
Current Sense Amplifiers





ADC Converter



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ADC CIRCUIT

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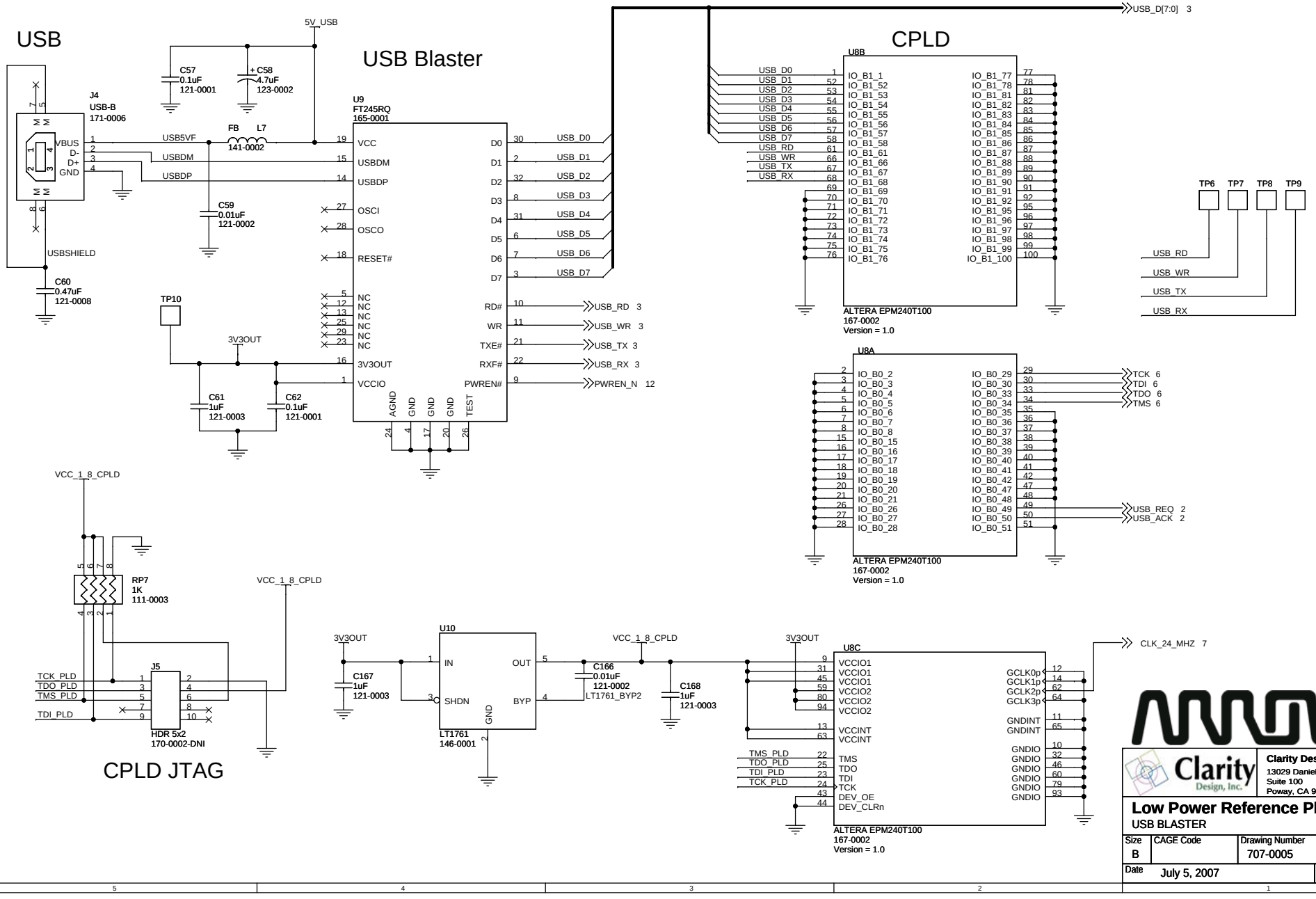
USB
USB Blaster
CPLD
5V_USB
J4
USB-B
171-0006
C57
0.1uF
121-0001
C58
4.7uF
123-0002
FB L7
141-0002
C59
0.01uF
121-0002
C60
0.47uF
121-0008
USBSHIELD
TP10
3V3OUT
C61
1uF
121-0003
C62
0.1uF
121-0001
U9
FT245RQ
165-0001
VCC
USBDM
USBDP
OSCI
OSCO
RESET#
NC
3V3OUT
VCCIO
AGND
GND
TEST
D0
D1
D2
D3
D4
D5
D6
D7
RD#
WR
TXE#
RXF#
PWREN#
USB_D[7:0] 3
USB_RD 3
USB_WR 3
USB_TX 3
USB_RX 3
PWREN_N 12
U8B
ALTERA EPM240T100
167-0002
Version = 1.0
TP6
TP7
TP8
TP9
U8A
TCK 6
TDI 6
TDO 6
TMS 6
USB_REQ 2
USB_ACK 2
VCC_1_8_CPLD
RP7
1K
111-0003
J5
HDR 5x2
170-0002-DNI
TCK_PLD
TDO_PLD
TMS_PLD
TDI_PLD
CPLD JTAG
U10
LT1761
146-0001
IN
SHDN
OUT
BYP
GND
C167
1uF
121-0003
C166
0.01uF
121-0002
LT1761_BYP2
C168
1uF
121-0003
U8C
VCCIO1
VCCINT
GCLK0p
GCLK1p
GCLK2p
GCLK3p
GNDINT
GNDIO
TMS
TDO
TDI
TCK
DEV_OE
DEV_CLRn
CLK_24_MHZ 7
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USB BLASTER
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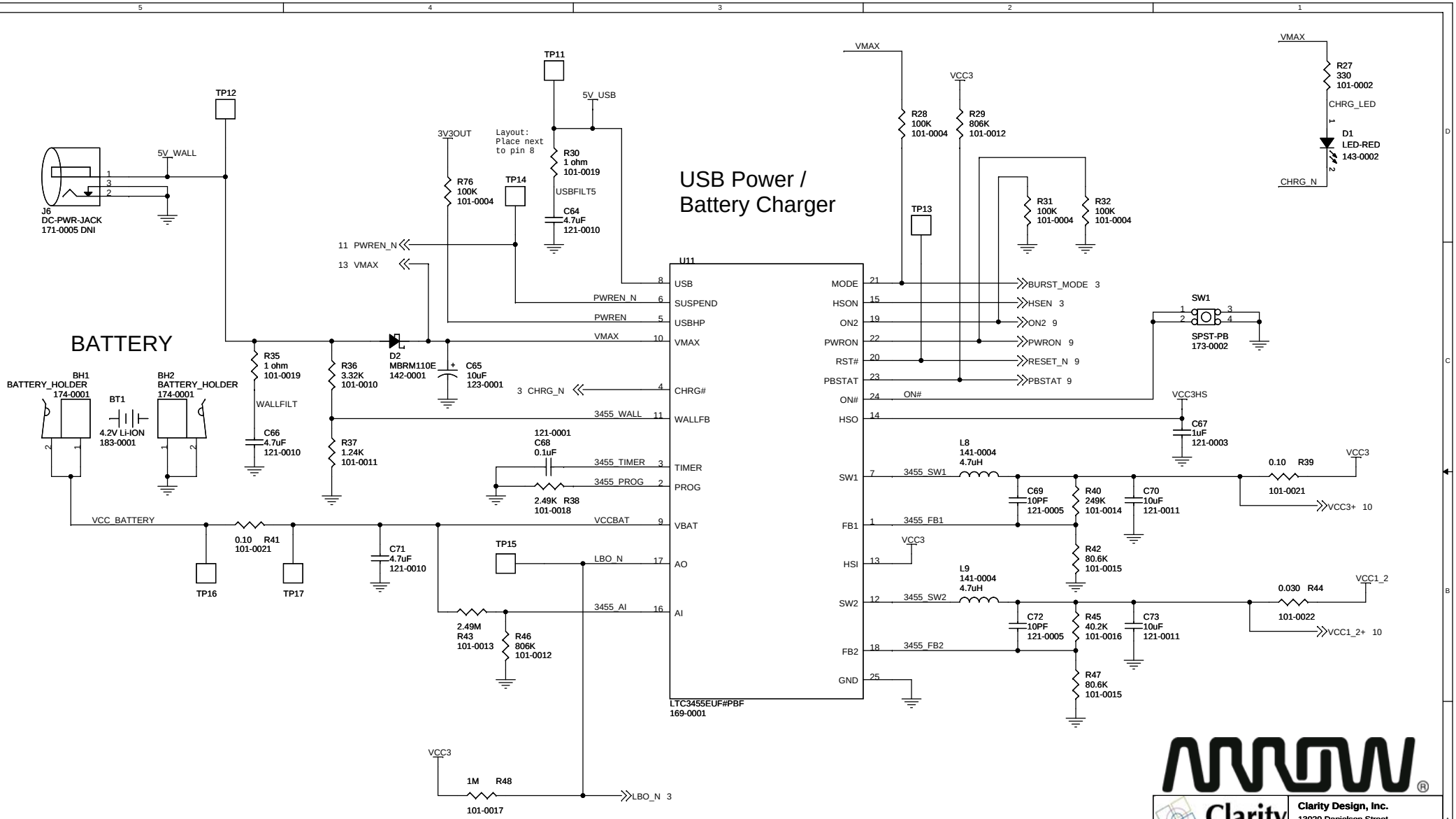

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USB POWER / BATTERY CHARGER

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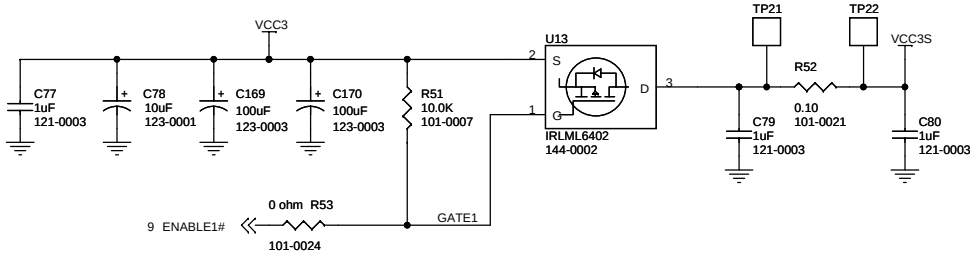
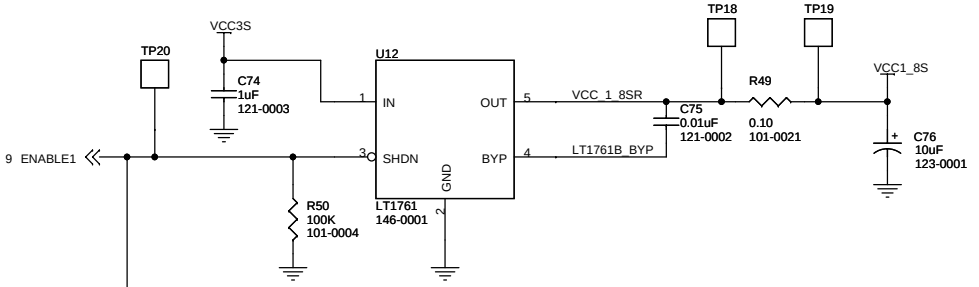
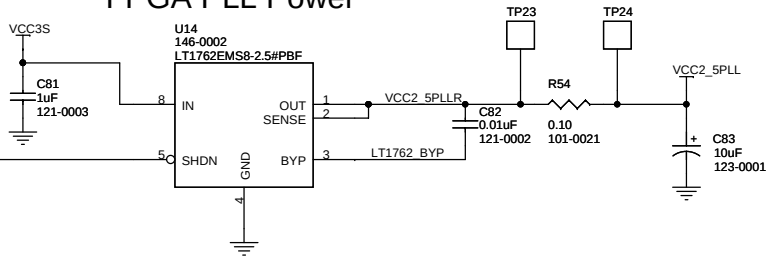
FPGA, Flash Power



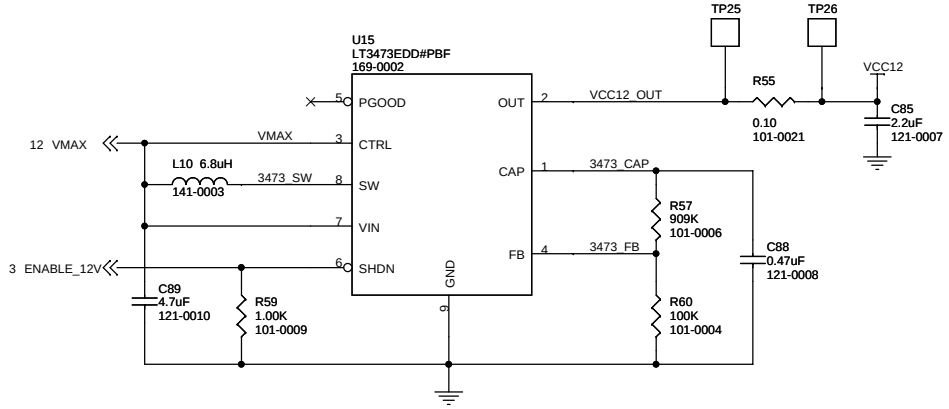
Flash, Audio, Display Power



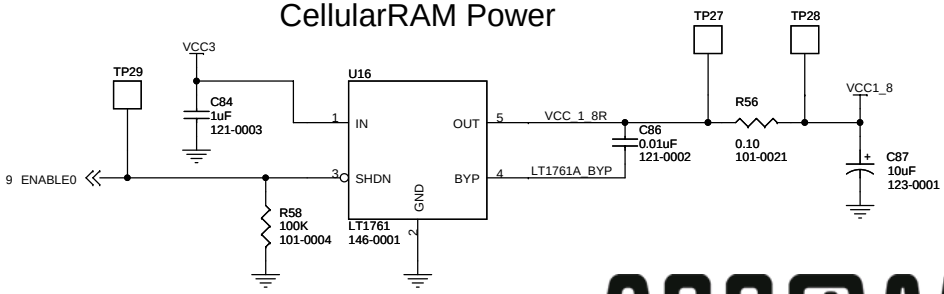
FPGA PLL Power



Display Power Supply



CellularRAM Power



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POWER

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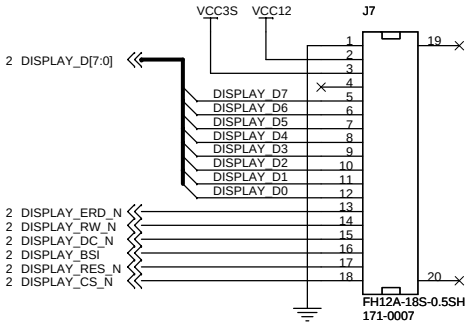
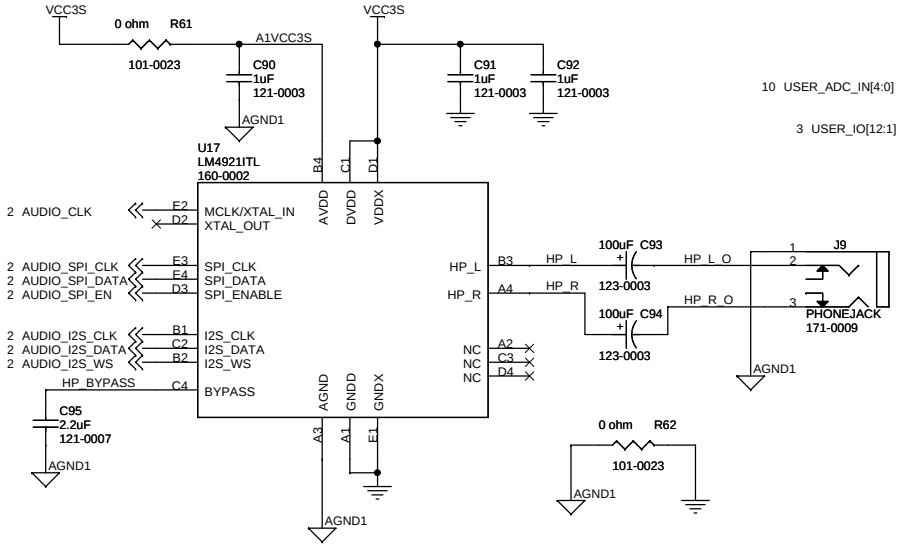
OSRAM OLED Display Connector

Note: Pin numbers for Connector are opposite to OSRAM OLED Data sheet. Check physical net connection for proper connectivity.

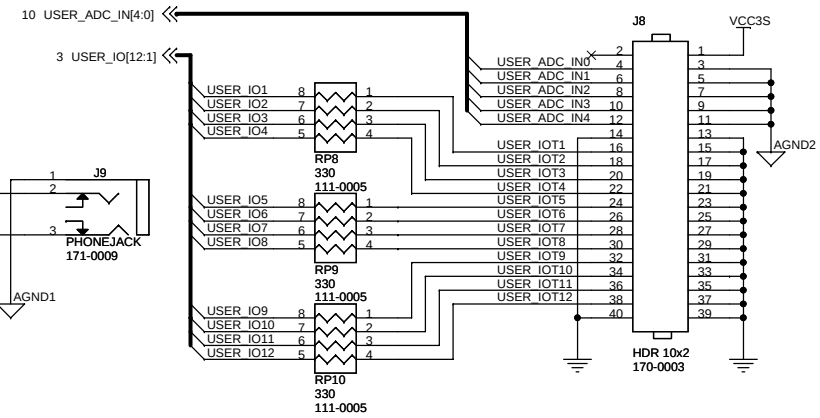


Note: J7 is top contact connector

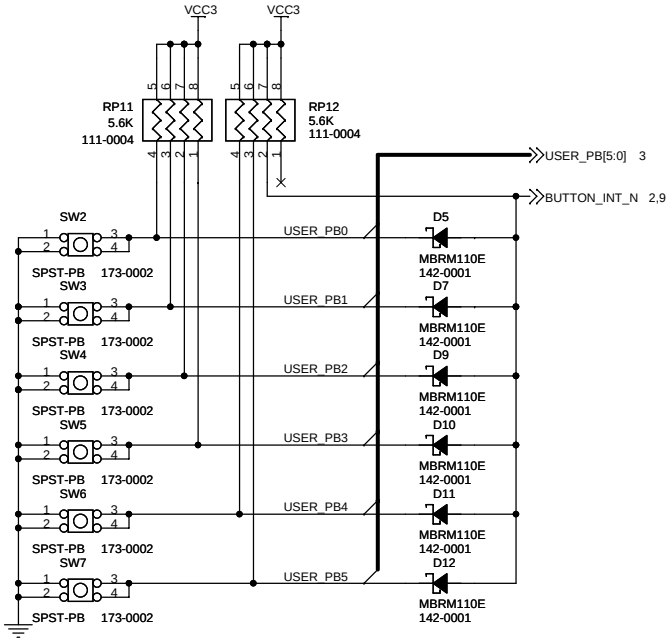
Headphone Driver



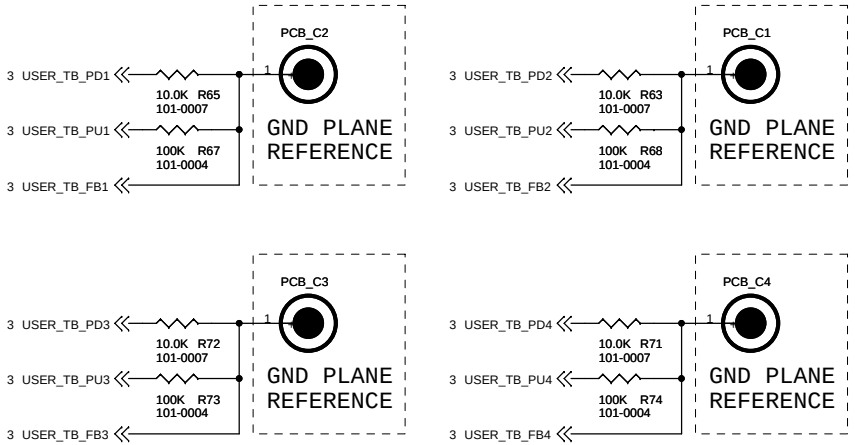
DEVELOPMENT HEADER



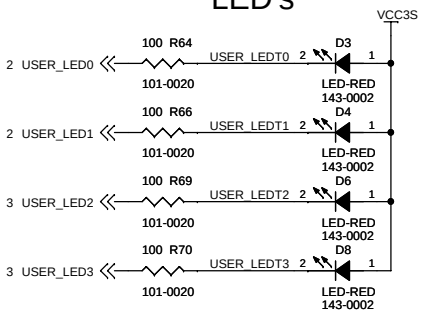
Buttons



Touch Sense Buttons



LED's



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Audio, Display, LED, I/O

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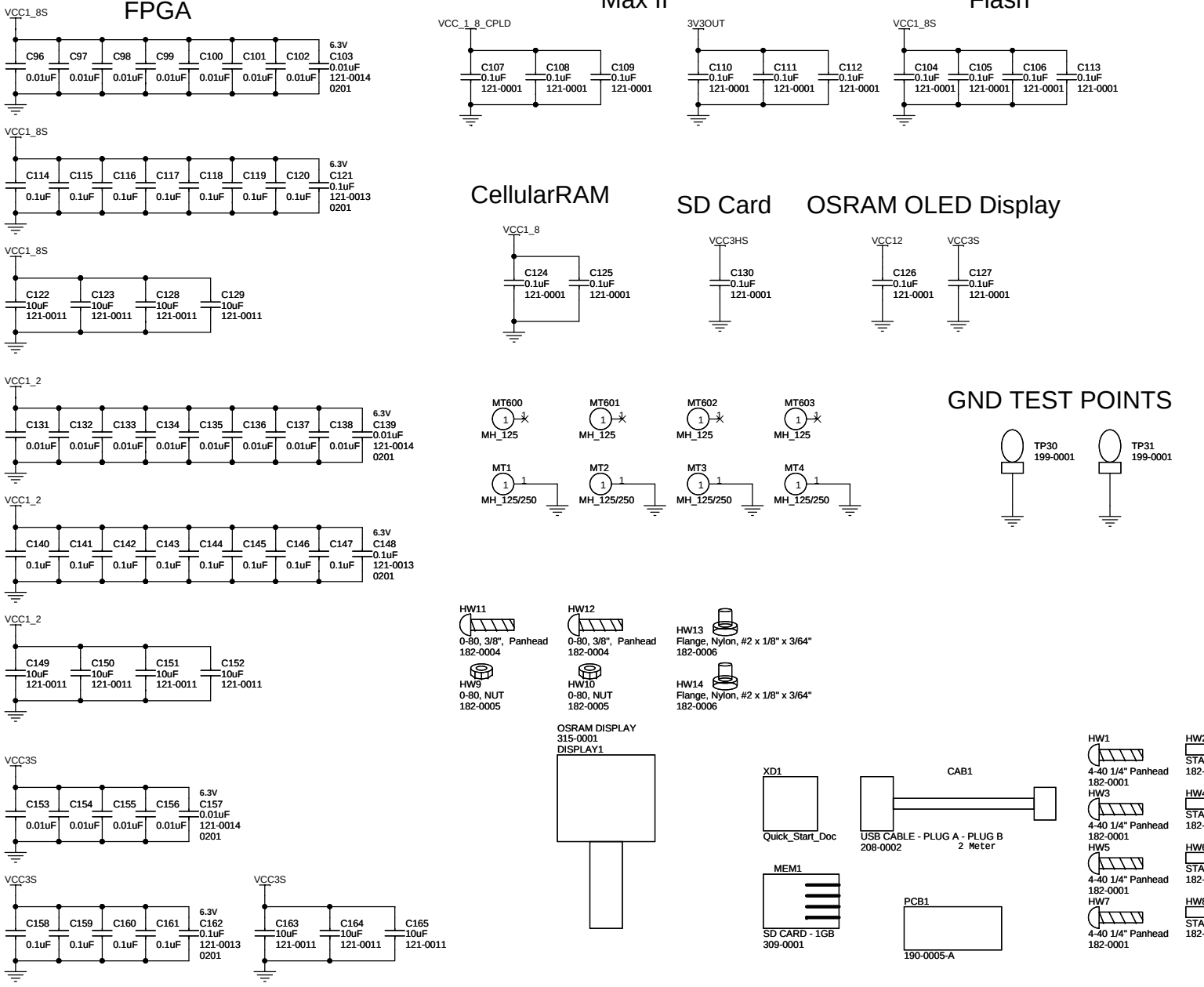

TESTPOINTS

TP1	NSTATUS
TP2	NCONFIG
TP3	CONF_DONE
TP4	CLK_48_MHZ
TP5	CLK_24_MHZ
TP6	USB_RD
TP7	USB_WR
TP8	USB_TX
TP9	USB_RX
TP10	3V3OUT
TP11	5V_USB
TP12	5V_WALL
TP13	RESET_N
TP14	PWREN_N
TP15	LBO_N
TP16	VCC_BATTERY
TP17	VCCBAT
TP18	VCC_1_8SR
TP19	VCC1_8S
TP20	ENABLE1
TP21	VCC3S-DRAIN
TP22	VCC3S
TP23	VCC2_5PLLR
TP24	VCC2_5PLL
TP25	VCC12_OUT
TP26	VCC12
TP27	VCC_1_8R
TP28	VCC1_8
TP29	ENABLE0
TP30	GND
TP31	GND

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DECOUPLING & MISCELLANEOUS

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